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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fernando Gonzalez et al.	§	Group Art Unit: 2815
Serial No.: 10/751,141	§	Examiner: Nguyen, Joseph H.
Filed: December 31, 2003	§	
For: Transistor Having Vertical Junction Edge and Method of Manufacturing the Same	§	Atty. Docket: MICS:0114 02-1010

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37 C.F.R. 1.8

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REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41 AND IN RESPONSE TO THE EXAMINER'S ANSWER MAILED MARCH 31, 2006

This Reply Brief is being filed pursuant to 37 C.F.R. § 41.41 in response to the Examiner's Answer mailed on March 31, 2006. Specifically, this Reply Brief addresses the Examiner's continual insufficiency and inconsistency of the Examiner's rejections based on the Michejda reference. Appellants respectfully ask that the Board carefully consider not only the points made in this Reply Brief, but also Appellants' complete argument set forth in the previously filed Appeal Brief (submitted to the Office on January 13, 2006).

Independent claims 12, 17 and 22 each recite, *inter alia*, a transistor comprising "a drain terminal comprising a doped polysilicon material *disposed within a first shallow cavity formed in an isolation oxide region*" and "a source terminal comprising a polysilicon material *disposed within a second shallow cavity formed in the isolation oxide region*." Emphasis added.